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Schwegman, Lundberg, Woessner & Kluth, P. A.
Attn: Dana B. LeMoine
P.O. Box 2938
Minncapolis, MN 55402

EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,175	PORTERFIELD, A. KENT	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,22-29 and 37-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,22-29 and 37-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is responsive to the amendment filed on February 3, 2006.

2. Claims 1-59 are pending. Claims 16-21 and 30-36 are cancelled.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 11, 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, applicant define a low-level software is a software routine from BIOS that executed by the processor to initialize the system and a higher level software such as an operating system. However, it is unclear to examiner that the claim limitation "the first level of software is ***lower than the second*** level of software" in what way is one level of software is lower than the other (figuratively, literally or in term of system level) .

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 6, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Mitra et al. (Mitra) U.S. Patent 6,167,472.

7. As per claim 6, Mitra discloses a PCI local bus compliant device comprising:

a hardware implemented capabilities list [col. 1 lines 37-39, col. 2 lines 64-67] capable of being modified by low level software [col. 4 lines 25-33; col. 9 lines 31-35], and read-only to higher level software [col. 2 lines 52-67].

8. As per claim 10, Mitra teach the compliant device comprises an integrated circuit that includes the hardware implemented capabilities list [col. 3 lines 7-19].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schimmel U.S. Patent 6,601,120 in view of Sibigtroth U.S. Patent 4,580,246.

12. As per claim 1, Schimmel discloses an apparatus comprising:

a hardware linked list, the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register [col. 7 lines 11-29] pointed to a capability/configuration supported by the device.

However, Schimmel does not explicitly teach a locking mechanism to conditionally make the next node pointer register of teach of plurality of nodes read-only.

Sibigtroth teaches another method related to a write protection circuit and method for a control register which allows a write protected register to be written only once [col. 1 lines 10-13]. Specifically, Sibigtroth teaches a locking mechanism to conditionally make the register read-only [fig. 3].

As taught by Sibigtroth, certain control registers and bits which determine system configuration would pose serious system integrity problems were they writeable, or under software control , during normal operation [col. 1 lines 14-17]. Therefore, it would have been obvious to one of ordinary skill in the art at time of the invention was made to have modified the system of Schimmel with the lock mechanism of Sibigtroth to conditionally make the next node pointer register of each of the plurality of nodes read-only.

The motivation for doing so would have been to prevent accidental write or modification to the linked list structure since an unintended modification to these registers could change the device configuration/capability resulting in a device failure [col. 1 lines 18-21].

13. As per claim 2, Sibigtroth teaches the locking mechanism comprises a control register [110 fig. 3].

14. As per claim 3, Schimmel teaches each of the plurality of nodes includes a register operable to specify a capability of the apparatus [col. 7 lines 11-29].

15. As per claim 4, Schimmel teaches the apparatus comprises a PCI local bus compliant peripheral device [inherent – col. 7 lines 11-13].

16. As per claim 5, Schimmel teaches the apparatus comprise an integrated circuit having a microprocessor bus compatible interface [inherent].

17. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carson et al. U.S. Patent 5,911,051 in view of Gafken U.S. Patent 6,026,016.

18. As per claim 6, Carson et al. teach a PCI local bus compliant device comprising:

a hardware implemented capabilities list [col. 42 lines 24-30] capable of being read-only to higher level software [col. 40 lines 35-39]. However, Carson et al. do not teach expressly the hardware implemented capabilities list capable of being modified by low-level software.

Gafken present another invention relates generally to a memory array and more particularly to a method and apparatus for locking and unlocking blocks of memory cells in a nonvolatile memory array to disable and enable write and erase. Specifically, Gafken teaches due to the nature of the locking mechanism of previous art, in order to update or make modification to the critical information in the memory, the user required to open up the system to physically change the setting to unlock the memory. Therefore, while system critical

information is protected in locked blocks, updates to such information can be difficult [col. 1 lines 28-58].

Gafken teaches, for ease of use and upgradeability, the desired locations in the memory arrays, which are read-only, are capable of being modified by low level software [col. 6 lines 38-44; col. 13 lines 5-34, 60-65];

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Carson et al. with a low-level software of Gafken in order to provide the system the abilities to modified the hardware capabilities list.

The motivation for doing so would have been to provide the system the ease of use and upgradeability of the capabilities list; and at the same time, to prevent inadvertent erasure or modification to critical information in the list [col. 14 lines 27-39].

19. As per claim 7, Carson et al. teach the hardware implemented capabilities list comprises a plurality of list nodes that each includes a next node pointer register [col. 42 lines 24-48]. Gafken teaches the method for modifying read-only register. Therefore, it is obvious to one of ordinary skill in the art that the combine teachings of Carson et al. and Gafken teach a writeable next node pointer register.

20. As per claim 8, Gafken teaches a control register [140 fig. 1] coupled to the writeable register [130 fig. 1], the control register being operable to change the writeable registers to read-only register [from col. 13 line 66 to col. 14 line 5; col. 14 lines 41-52]. Therefore, it is obvious to one or ordinary skill in the art that the combine teachings of Carson et al. and Gafken also

teach a control register being operable to change the writeable next node pointer register to read-only.

21. As per claim 9, Carson et al. teach the hardware implemented capabilities list is read-only to operating system software [see claim 6] and Gafken teaches writeable by basic input output software [col. 6 lines 38-44; col. 13 lines 5-34, 60-65].

22. As per claim 10, Carson et al. teach the PCI local bus compliant device comprises an integrated circuit that included the hardware implemented capabilities list [col. 40 lines 35-45 and col. 42 lines 1-9].

23. Claim 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen et al. U.S. Patent 6,154,819 in view of Schimmel.

24. As per claim 11, Larsen et al. teach an integrated circuit comprising:

an address bus [inherent – fig. 1, 7];

a data bus [inherent – fig. 1, 7];

a control bus [fig. 2, 3];

a series of memory array blocks coupled to the address, data, and control busses, the series of memory array blocks arranged in a writeable list [col. 1 lines 37-40; 202 fig. 2];

a control register [116, 206 fig. 2] operable to lock the writeable memory array blocks and conditionally make the series of memory blocks read-only [col. 4 lines 12-16; col. 7 lines 37-53]; and

wherein the control register is accessible by a first level of software[1] [204 fig. 2; col. 5 lines 7-8; col. 7 lines 37-40] and the series of memory array blocks are inherently accessible by a second level of software [col. 11 lines 45-51], wherein [it is obvious] the first level of software is lower than the second level of software.

However, Larsen et al. do not teach the memory array blocks are arranged as a linked list.

Schimmel teaches another integrated circuit having a storage spaces for storing the device's capabilities. Specifically, Schimmel teaches the storages spaces arranged in a series of linked list registers [col. 7 lines 11-29].

At the time of the invention was made, it would have been obvious a person of ordinary skill in the art to have modified the system of Larsen et al. with a linked list data structure as taught by Schimmel since Larsen et al. do not explicitly prohibit the use of linked list and linked list, which allows for rapid insertion and removal of the elements in the linked list without having to move or relocate large blocks of physical memory, is such a well know data structure for storing information.

25. As per claim 12, Schimmel teaches the series of linked list registers are arranged in groups, each group forming a linked list node, each linked list node including one next node pointer register [col. 7 lines 22-34].

[1] First level-software or low-level software by definition is a software which handles the interface to peripheral hardware.

26. As per claim 13, the combine teachings of Schimmel and Larsen et al. inherently teach the control register is operable to make the next node pointer register of each linked list node read-only.

27. Claim 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley et al. US 2002/0073258 in view of Larsen et al U.S. Patent 6,154,819.

28. As per claim 15, Riley et al. teach an integrated circuit comprising:

an address bus [paragraph 0285];

a data bus [paragraph 0285];

a control bus [paragraph 0630];

a series of linked list register [paragraph 0676-0677] coupled to the address, data, control busses [paragraph 0669-0670], a series of linked list registers arranged in a readable linked list and configured as read-only. However, Riley et al do not explicitly teach that the series of linked list registers are writeable nor a control register operable to lock the writeable linked list and conditionally make the series of linked list register read-only.

Larsen et al. teach another device comprises a serious of writeable memory array usable to store upgradeable configuration information [col. 1 lines 39-41] wherein the serious of register [202 fig. 2] coupled to the address, data [fig. 7], and control busses [fig. 3]. Specifically, Larsen et al. teach a control register [col. 4 lines 14-16, 56-67] operable to lock the writeable series of writeable memory array and conditionally make the series of lined list register read-only [abstract, col. 7 lines 33-54].

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to have modified the system of Riley et al. with a series of writeable register (memory array) and a control register operable to lock and conditionally make the serious of register read-only as taught by Larsen et al.

The motivation for doing so would have been to provide the system the ability to upgrade or reprogram the information stored in the plurality of the registers; and at the same time, protect the information from unintended erasure or reprogramming as teach by Larsen et al. [col. 1 lines 39-43; 56-59; col. 2 lines 62-65].

29. As per claim 14, Larsen et al. teach the control register is accessible by a first level of software [col. 7 lines 37-40] and Riley et al. inherently teach the series of linked list registers are accessible by a second level of software, wherein it is obvious that the first level of software is lower than the second level of software.

30. Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schimmel in view of DeRoo et al. U.S. Patent 5,764,995.

31. As per claim 22, Schimmel teaches an integrated circuit comprising:

a first register to signify whether a capabilities list is enabled [col. 7 lines 20-22];

a second register to point to a capabilities list [col. 7 lines 22-24];

However, Schimmel does not explicitly teach a first and second register as a writeable register and a write-once control register operable to make the first and second writeable register read-only.

DeRoo et al. teach another integrated circuit comprising plurality of writeable registers for storing plurality of configuration [col. 2 lines 28-34]. Specifically, DeRoo et al. teach a write-once control register operable to make the plurality of writeable register read-only [claim 1; col. 2 lines 39-47].

At the time of the invention was make, it would have been obvious to one of ordinary skill in the art to have modified to system of Schimmel with a writeable register and a write once control register of DeRoo et al. to make the first and second writeable registers read-only.

The motivation for doing so would have been to provide the system the ability to modify/reprogram the specific configuration in the registers without having manually reconfigured [from col. 1 line 60 to col. 2 line 26] and prevent unintended erasure during the normal operation of the system.

32. As per claim 23, DeRoo et al. teach the control register can be written only once between system resets [claim 1].

33. As per claim 24, Schimmel teaches a hardware linked list pointed to by the second writeable register, the hardware linked list including a plurality of nodes [col. 7 lines 20-24]. And DeRoo et al. teach a writeable register to provide the system the ability to reprogram the specific information in the register.

34. As per claim 25, the combine teaching of Schimmel and DeRoo et al. inherently teach the control register operable to make the writeable next node register read-only.

35. As per claim 26, Schimmel teaches a PCI local bus compliant interface [col. 7 lines 11-13].

36. Claims 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al U.S. Patent 5,999,198 in view of Lin et al U.S. Patent 5,765,026 and DeRoo et al.

37. As per claim 27, Horan et al teach an integrated circuit comprising:

a hardware linked list of register containing information for each capability supported by a peripheral device. Horan et al teach a group of register operable to indicate the capabilities of the integrated circuit. However, Horan et al do not teach expressly a plurality of register group.

Lin et al teach another method for creating a plurality of linked lists, wherein the method includes the step of retrieving a single selected portion of the combination of information from a linked list. Specifically, Lin et al teach a plurality of register groups, each register group including registers operable to indicate the state information of a system [col. 1 lines 43-48; col. 3 lines 22-27; col. 4 lines 12-27], and including a next group register to point to a next group [fig. 4].

Horan et al and Lin et al are analogous art because they from the same field of endeavor – Data management in memory.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Horan et al with the plurality of linked list (group of register), each linked list including register operable to indicate the state information of the system as taught Lin et al to manage the different capabilities in a peripheral device.

The suggestion/motivation for doing so would have been to improve the access speed and reducing the storage requirement in a memory [col. 1 lines 29-32].

However, the combine teachings of Horan et al. and Lin et al. do not teach a control register operable to renders the plurality of register groups read only and a write once lock bit is configured such that the write-once lock bit can be written to only once between system reset sequences.

DeRoo et al. teach another integrated circuit comprising plurality of writeable registers for storing plurality of configuration. Specifically, DeRoo et al. teach the control register comprises a write-once lock bit [col. 82 lines 29-45], that when written, renders the plurality of register read-only and the write once lock bit is configured such that the write-once lock bit can be written to only once between system reset sequences [claim 4].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Horan et al. and Lin et al. with a control register comprises a write-once lock bit of DeRoo et al. to renders the plurality of register groups read-only.

The motivation for doing so would have been to provide a means to modify or reprogram the groups of registers once but only under controlled condition [abstract].

Therefore, it would have been obvious to combine Horan et al. with Lin et al. and DeRoo et al. to obtain the invention as specified in claim 27.

38. As per claim 28, Horan et al/Lin et al teach the plurality of register groups [Lin et al] form a PCI local bus compliant capabilities list [Horan et al –col. 17 lines 1-19].

39. As per claim 29, DeRoo et al. teach the control register is modifiable once by basic input output software, and is not modifiable by operating system software [col. 2 lines 37-39; col. 81 lines 45-48].

40. Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schimmel in view of Larsen et al.

41. As per claim 1, Schimmel teaches a computer system comprising:

a PCI local bus compliant peripheral device coupled to a bus [102 fig. 1]; and

a processor [101 fig. 1] coupled to the bus;

wherein the PCI local compliant peripheral device includes a capabilities linked list [col. 7 lines 22-26].

However, Schimmel does not explicitly that the capabilities linked list is modifiable by the processor, and wherein the PCI local bus compliant peripheral device further includes a writeable control register operable to render the capabilities linked list read-only by the processor.

Larsen et al. teach another device comprises a serious of writeable memory array usable to store upgradeable configuration information [col. 1 lines 39-41] wherein the serious of register [202 fig. 2] coupled to the address, data [fig. 7], and control busses [fig. 3]. Specifically, Larsen et al. teach a control register [col. 4 lines 14-16, 56-67] operable to lock the writeable series of writeable memory array and conditionally make the series of lined list register read-only [abstract, col. 7 lines 33-54] by the processor [see further discussion in claim 15].

42. As per claim 38, Schimmel teaches the capabilities linked list comprises a plurality of nodes made up of groups of registers, each node corresponding to one capability and including one next node pointer register [see claim 35] and Larsen et al. teach a writeable register.

Therefore, At the time of the invention was make, it would have been obvious to one of ordinary skill in the art that the combine teachings of Schimmel and Larsen et al. included the claim the writeable next node pointer register.

43. As per claim 39, the combine teaching of Schimmel and Larsen et al. inherently teach render the writeable next node pointer registers read-only.

44. As per claim 40, Larsen et al. teach a memory device having processor instructions stored therein, the processor instructions being operable to cause the processor to write to the writeable control register [from col. 3 line 62 to col. 4 line 11; col. 7 lines 37-41].

45. As per claim 41, Schimmel teaches the PCI local bus compliant peripheral device includes register to indicate whether the capabilities linked list is enabled [col. 7 lines 20-22]. However, Schimmel does not explicitly teach that the register is writeable. Larsen et al teach a programmable series of memory array blocks such that it would have been obvious to one of ordinary skill in the art that the combine teachings of Schimmel and Larsen et al. included the claimed writeable register.

46. Claims 42-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schimmel in view of Gafken U.S. Patent 6,026,016.

47. As per claim 42, Schimmel teaches a hardware linked list comprising:

a first list node having a capabilities register and a next node pointer register; and

a second list node having a capabilities register and a next node pointer register [col. 7 lines 22-34];

Schimmel does not teach a control register, and in response to the control register, the next node pointer registers of the first and second list nodes are conditionally read-only.

Gafken teaches a method for controlling locking and unlocking of a block in a memory array. Specifically, Gafken teaches a control register [137, 135, 140 fig. 1] and wherein the plurality of blocks in the memory array are conditionally made read-only in response to the control register [col. 6 lines 38-44].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Schimmel with the control register of Gafken to conditionally made the next node pointer registers of the first and second list nodes read-only.

The motivation for doing so would have been to prevent inadvertent overwriting or other undesired alteration to the linked list which would compromise the device integrity.

48. As per claim 43, Schimmel teaches a head pointer register to point to the first list node and Gafken teaches a writeable register wherein the writeable register are conditionally read-only in response to the control register. Therefore, it is obvious to one of ordinary skill in the art that

the combine teachings of Schimmel and Gafken teach the writeable head pointer register being conditionally read-only in response to the control register.

49. As per claim 44, Schimmel teaches the hardware linked list is compliant with a PCI local bus rev. 2.2 capabilities list [col. 40 line 42].

50. As per claim 45, Gafken teaches the control register is a write-once register [from col. 7 line 64 to col. 8 line 5].

51. As per claim 46, Gafken teaches the control register can be written to only once between hardware resets [see claim 45; col. 10 lines 47-52].

52. As per claim 47, Schimmel teach a method of initializing a computer peripheral comprising:

during initialization of the computer peripheral, the computer system communicates with the peripheral to obtain a list of capabilities stored in a hardware linked list within the peripheral.

Schimmel does not expressly teach the writing a list of capabilities to nodes in a hardware linked list. Particularly, Schimmel does not teach that the system have the ability to modify the linked list or teach a control register within the computer peripheral to made the nodes read-only.

Gafken present another invention relates generally to a memory array and more particularly to a method and apparatus for locking and unlocking blocks of memory cells in a

nonvolatile memory array to disable and enable write and erase. Specifically, Gafken teaches due to the nature of the locking mechanism of previous art, in order to update or make modification to the critical information in the memory, the user required to open up the system to physically change the setting to unlock the memory. Therefore, while system critical information is protected in locked blocks, updates to such information can be difficult.

Gafken teaches, during the initialization of the computer peripheral [115 fig. 3-memory module], the writing/re-programming of the desired location in the memory array [515 fig. 5; col. 13 lines 59-65] and to a control register [315 fig. 3] within the computer peripheral to make the location of memory array read-only [from col. 13 line 66-3].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Schimmel with the ability to modified the location of memory array [register] of Gafken to write a list of capabilities to nodes in a hardware linked list and a control register taught by Gafken to make the nodes read-only.

The motivation for doing so would have been to provide the system the ease of use and upgradeability of the list of capabilities to node in a hardware linked list; and at the same time, to prevent inadvertent erasure or modification to the linked list.

53. As per claim 48, Gafken teaches the method for altering the information a desire location of the memory. Therefore, it is obvious to one of ordinary skill in the art that the combine teachings of Schimmel and Gafken teach the modifying to the next node pointer register.

54. As per claim 49, Gafken teach writing to a control register comprises writing once to a capabilities lock bit, which thereafter is read-only [see claim 45-46].

55. As per claim 50, Schimmel teaches a capabilities list enabled register [col. 7 lines 20-21] and Gafken teaches the system with the ability to modify a read-only register. Therefore, it is obvious to one of ordinary skill in the art that the combine teaching of Schimmel and Gafken teach the writing to a capabilities list enabled register.

56. As per claim 51, Gafken teaches the method is performed by basic input output software prior to loading of an operating system [fig. 5]

57. As per claim 52, Schimmel teaches a method of initializing a PCI local bus compliant device comprising:

reading a link within a capabilities linked list in the PCI local bus compliant device. However, Schimmel does not teach reading instructions from a memory device holding basic input output software to modify a link within a capabilities linked list and writing to a control register in the PCI local bus compliant device to make the link read-only.

Gafken present another invention relates generally to a memory array and more particularly to a method and apparatus for locking and unlocking blocks of memory cells in a nonvolatile memory array to disable and enable write and erase. Specifically, Gafken teaches due to the nature of the locking mechanism of previous art, in order to update or make modification to the critical information in the memory, the user required to open up the system to

physically change the setting to unlock the memory. Therefore, while system critical information is protected in locked blocks, updates to such information can be difficult.

Gafken teaches, during the system initialization, reading instruction from a memory device holding basic input output software [151 fig. 1; col. 13 lines 26-40];

modifying a desired locations in the memory array within the memory module[col. 13 lines 62-63]; and

writing to a control register in the memory module to make the location in the memory array read-only [from col. 13 line 66 to col. 14 line 2].

At the time of the invention was make, it would have been obvious to one of ordinary skill in the art to have modified to system of Schimmel with the reading instruction from a memory device holding BIOS software as taught by Gafken to modify a link within a capabilities linked list in the PCI local bus compliant device in the Schimmel system and a control register taught by Gafken to make the link read-only,

The motivation for doing so would have been to provide ease of use and upgradeability of the link within the linked list; and at the same time, to prevent inadvertent erasure or modification to the linked list [col. 14 lines 27-40].

58. As per claim 53, the examiner takes Official Notice of the fact that the manipulation of the linked list is an old and well-know method.

59. As per claim 54-55, Gafken teaches the system with the ability to modify a read-only register. Therefore, it is obvious to one of ordinary skill in the art that the combine teaching of

Schimmel and Gafken teach the writing to a capabilities list enabled register and to a head pointer register in order to modify the capabilities list.

60. As per claim 56, Schimmel teach an apparatus having a computer readable medium with machine-readable instructions for a method stored thereon, the method comprising:

reading a next node pointer register in a PCI local bus peripheral to indicate the existence of a capability [col. 7 lines 20-22].

However, Schimmel does not teach the modifying a next node pointer register or a control register to make the next node pointer register read-only.

Gafken teach another method for modifying a location in a memory [register]; and

the modifying a control register to make the next node pointer register read-only [see discussion in claim 52].

61. As per claim 57, Schimmel teaches a head pointer register to point to a hardware linked list. Gafken teaches the system with the ability to modify a protected register and, after modify, re-lock the register to render the register read-only responsive to the control register. Therefore, it is obvious to one of ordinary skill in the art that the combine teaching of Schimmel and Gafken teach the modifying of a head pointer register to a hardware capabilities linked list, wherein the head pointer become read-only responsive to the control register.

62. As per claim 58, Gafken teach the apparatus comprises a read-only memory [abs]

63. As per claim 59, see claim 50.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Vincent Tran